Specification
eBUS Conformance Testing

Physical Layer Testing

Asynchronous Mode
Version 1.0 / 22.10.1998
Ref eBUS Specification Layer 1 / 2, Vers 1.1.1

1 Contents

2 Introduction

This document specifies the tests necessary to check the conformance of bus timing and technical interface to eBUS Specification layer 1 / 2 , vers 1.0 .
This document does not consider the synchronous mode.

2.1 Overview: The Tests

The eBUS physical layer tests can be subdivided into four groups:

- test cases concerning the bus timing
- test cases concerning the technical interface
- test cases concerning the eBUS power supply
- test cases concerning the AUTOSYN generator

The table below gives a survey of the tests:

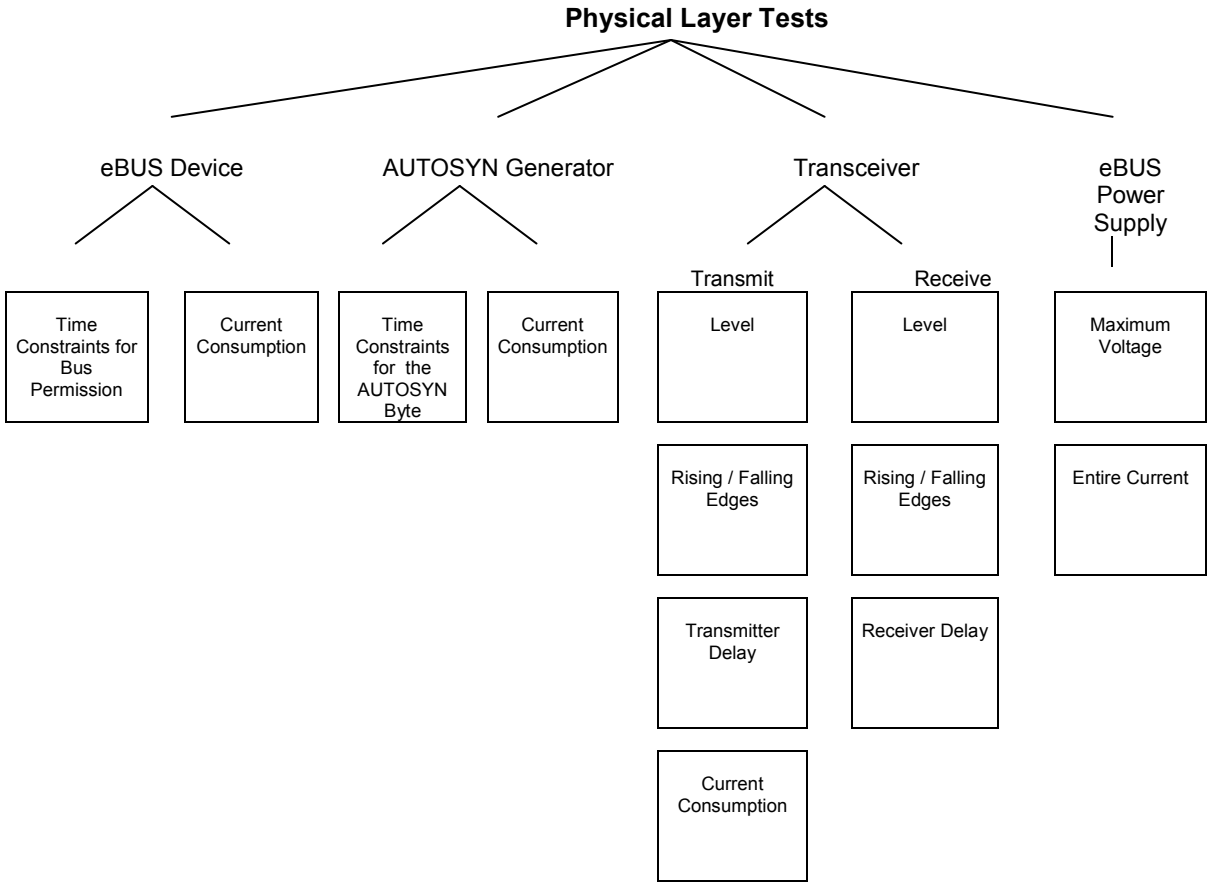


fig. 1 : survey of the physical layer tests

Depending on the respective realization of the devices and parts of devices mentioned in fig. 1 there may be some conditions to be fulfilled or some restrictions concerning the tests. Have a look at the check list in the appendix (chapter 7.1).

2.2 Test Environment

2.2.1 Common Overview

The following figure shows the main components of the test environment in an abstract way:

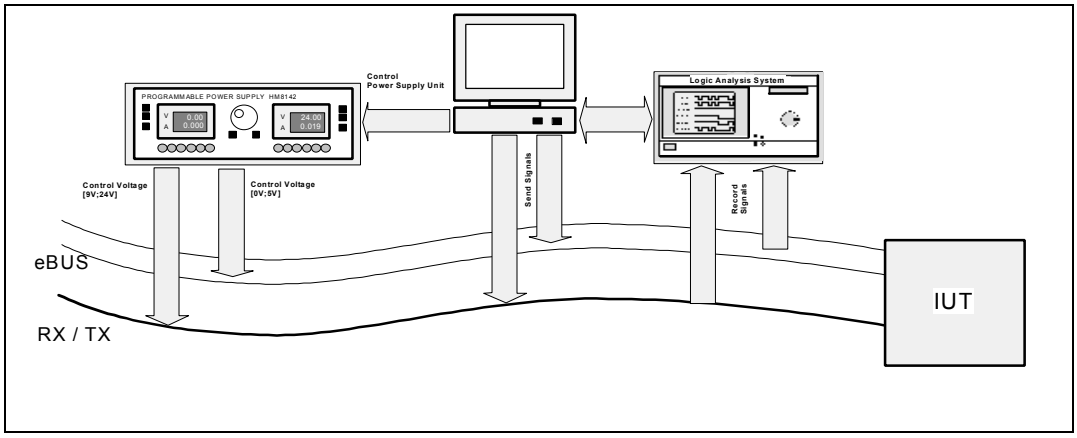


fig. 2 : main components of the test environment

The group of components which are needed to realize test execution will be hereafter referred to as Lower Tester (LT).

The main components of the LT are:
- PC for
  - initializing logic analyser (LSA) / oscilloscope
  - running and stopping logic analyser / oscilloscope
  - sending and receiving signals
  - checking and verifying measure results
- logic analyser / oscilloscope (logic analysis system)
- circuit board

For programming the tests and controlling the devices LabView is used. For some tests LabView uses dynamic link libraries written in C and Delphi.

Depending on the implementation to be tested different parts of the LT are used for a test.
A figure at the beginning of the description of each test case will show you the respective components.

The following implementations can be tested (IUT):
- eBUS transceiver
- AUTOSYN generator
- eBUS device
- eBUS power supply

2.2.2 Technical Informations

The following devices and boards are used for the tests:

- HM8142 power supply unit
  setting accuracy : 0.2% of value ± 3 digit
- HP16500C logic-analysis-system (LSA)
  - oscilloscope:
    Time Interval Measurement Accuracy:
    ± [(0.005% of delta t)+(2 x $10e^{-6}$ x delay setting) + 100 ps] (maximum sample rate)
    ± [(0.005% of delta t)+(2 x $10e^{-6}$ x delay setting) + 0.15 x (1/sample rate)] (lower sample rate)
    Voltage Measurement Accuracy:
    ± (1.25% of full scale + offset accuracy + 0.016 V/div)
    DC Offset Accuracy:
    ± (1.0% of channel offset + 2.0% of full scale)
  - logic analyser:
    Sample Period Accuracy:
    0.01% of sample rate
    Time Interval Accuracy;
    ± (sample period + channel-to-channel skew + 0.01% of time interval reading)
    Channel-to-Channel Skew:
    2 ns, typical
- eBUS power supply 24VAC/DC 100mA
- GPIB NI-488.2
- special circuit board (test box)

When starting the tests several manual settings must be done before – depending on the respective test which will be executed. Instructions concerning these manual settings will be given on the monitor during execution of the tests.

2.2.3 Basic Adjustments

- Link up COM2 → transceiver and test box.
- Link up COM3 (PC) and test box.
- Link up LPT (PC) and test box.
- Link up GPIB (PC) and logic analysis system.
- Link up GPIB (PC) and power supply unit.
- Link up LSA and POD(test box).
- Link up BNC plug and test box.

2.3 Test Case Organisation

Each test case consists of three states:

- Set Up State
- Test State
- Verification State

2.3.1 Set Up State

The components of the test environment have to be in a certain set up state before running the test. The definition of this state may differ depending on the respective test case.
An explanation is given at the beginning of the specification of every test case.

2.3.2 Test State

This is the state in which the test is running: for example signals are sent or received and the respective values which should be tested are measured or are calculated from measured values.

2.3.3 Verification State

The LT verifies whether the test results corresponds with the specified and therefore expected values.

2.4 Test Case Description

The description of each test case is structured as follows:

- number and name of the test case
- the respective IUT
- a figure which shows the test environment
- test purpose
- a table with the respective definitions of the three test states (set up state – test state – verification)
- test analysis and test results: number of repetitions, expected result according to specification, respective accuracy
- additional informations

2.5 Test Results

Each test is iterated several times. The respective number of iterations is given in the table 'test analysis and test results' in the description of each test case. The test results are documented in a test report with one final test verdict for every test case.
In case of physical layer tests there are two possible verdicts:

- pass: the result of each iteration is in the permitted range
- fail : a test is failed if one or more test result(s) differ from the permitted range

The test report contains the following data for each test case:

- test verdict (pass / fail)
- number of iterations
- mean of measured data
- minimum value of measured data
- maximum value of measured data
- respective accuracy

Test Report

Tuesday, December 08, 1998 02:25 PM

Ref eBUS Specification Layer 1/2, Vers 1.1

eBUS - Transceiver

Static Test:

Current Consumption:

	high level		low level		
mean	0.00	mA.	0.00	mA.	
maximum	0.00	mA.	0.00	mA.	
minimum	0.00	mA.	0.00	mA.	Result: Warning

Accuracy: +/- 0,019 mA Expected: | low pegel <= | high level <= | low level + 10%

RX Level Test:

RX : threshold value from high to low level eBUS= 0.00 V.
RX : threshold value from low to high level eBUS= 0.00 V.
Accuracy: +/- 0,464 V

RX high level =	0.0 V	
RX low level =	0.0 V	Result: Fail

Accuracy: +/- 0,159 V Expected: 0 <= low <= 0.5, 2.5 <= high <= 5

TX Level Test:

eBUS : threshold value from high to low level TX = 0.00 V.
eBUS : threshold value from low to high level TX = 0.00 V.
Accuracy: +/- 0,159 V

eBUS low level =	0.00 V.	
eBUS high level =	0.00 V.	Result: Fail

Accuracy: +/- 1,414 V Expected: 9 <= low <= 12, 15 < high <= 24

Dynamic Test:

TX:

rising edges	0.00 µs	Result: Warning
falling edges	0.00 µs	Result: Warning
delay time	0.00 µs	Result: Warning

Accuracy: +/- 0,4 µs Expected: rise / fall time <= 5µs, delay <= 20µs

RX:

rising edges	0.00 µs	Result: Warning
falling edges	0.00 µs	Result: Warning
delay time	0.00 µs	Result: Warning

Accuracy: +/- 0,4 µs Expected: rise / fall time <= 5µs, delay <= 20µs

fig. 3 : test report - example

3 eBUS Device

3.1 Static Test Current Consumption

This test is only useful if the AUTOSYN generator is realized as a separate device.

IUT:
eBUS device

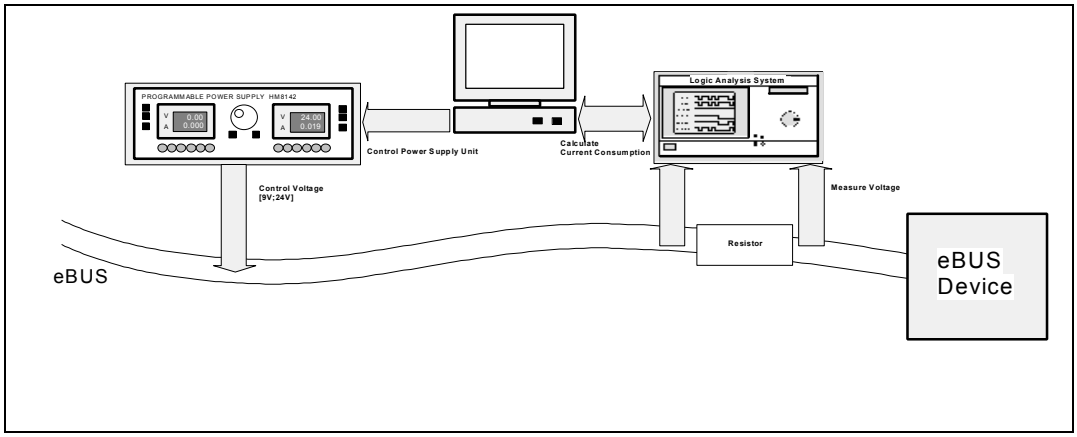


fig. 4 : current consumption of the BUS device – used components of test environment

Purpose:
testing current consumption:
current consumption (low) ≤ current consumption (high) ≤ current consumption (low) + 10%

State	Description
Set Up State	• eBUS power supply is adjusted to 9 V and the respective value given at the eBUS power supply unit (30mA ≤ I ≤ 100mA) • no signals on eBUS • oscilloscope is initialized • oscilloscope is running
Test State	REPEAT IF measured voltage is in a specified range • oscilloscope records voltage • increment voltage UNTIL measured voltage is > 24V • PC calculates current consumption values from measured voltage values
Verification	• PC calculates CCL and CCH from extremes of measured values • calculated results should be: CCL ≤ CCH ≤ CCL + 10%

The test:

Lower Tester	Flow	IUT eBUS Device
Set Up State according to definition above reached REPEAT OSC_Measures_Voltage PC_Calculates_Curr_Cons(Voltage) INC_eBUS_Voltage UNTIL eBUS_Voltage ≥ Maximum PC_Calculates_Curr_Cons_L PC_Calculates_Curr_Cons_H PC_Checks(Calculated_Curr_Cons_L, Specified_Curr_Cons_L) PC_Checks(Calculated_Curr_Cons_H, Specified_Curr_Cons_H)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	CCL ≤ CCH ≤ CCL + 10%	Accuracy for voltage: 1,25% of full scale = 0,0125 · 4V + 0,016V / Div = 0,016V · 4 = 0,064 = 0,114V Accuracy for current consumption: 0,633mA

Additional informations:

The basic idea of this test is to measure the voltage at a certain point (measure point voltage, see sketch page 6) against grounding.
Depending on the law of Ohm and the fact that there is a resistor of 180Ω the current consumption can be calculated from the measured voltage in the following way:

$$U = R \cdot I \Rightarrow I = \frac{U}{R} \Rightarrow current\ consumption = \frac{measure\ result}{180\ \Omega}$$

For the verification the following values are taken from the measured values:
CCL = smallest value from the measured values which are specified as low level
CCH = biggest value from the measured values which are specified as high level

As a special result this test provides the value of the closed circuit consumption. For the eBUS system closed circuit consumption is defined as the current consumption of all nodes at high level.
Because in the given environment there is just one node the result for current consumption at high level is equivalent to the closed circuit consumption.

3.2 Dynamic Test Time Constraints for Bus Permission

IUT:
eBUS device

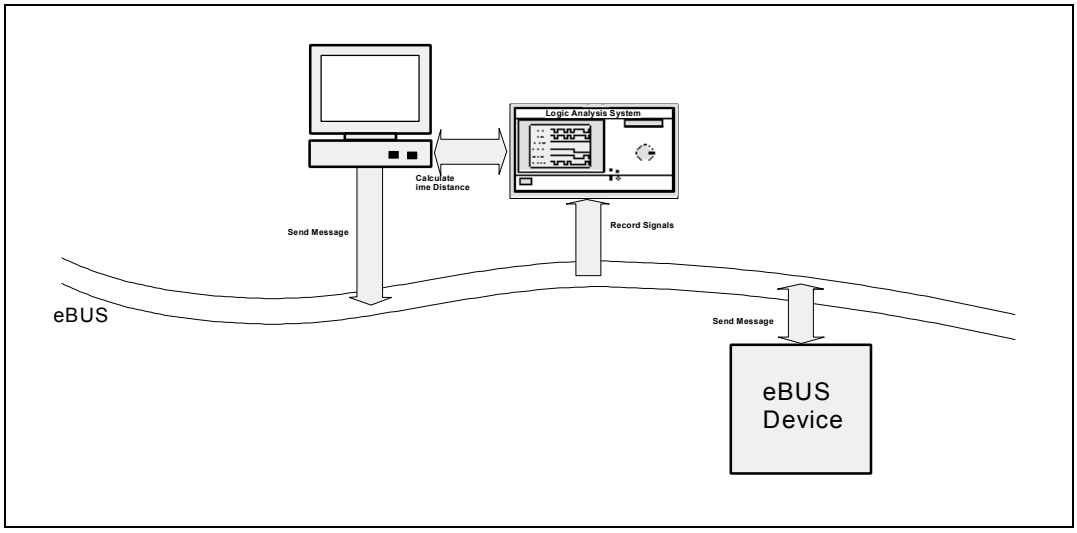
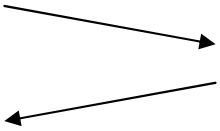


fig. 5 : bus permission - used components of test environment

Purpose:
testing time distance between start bit of SYN byte and bus permission of the eBUS device:
4300µs ≤ time distance ≤ (4300 + 156,24)µs
testing whether (416,17 – 1,2%)µs ≤ length of the start bit after SYN Byte ≤ (416,17 + 1,2%)µs

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • no traffic on eBUS • AUTOSYN generator is enabled • LSA is initialized • LSA is running • sample rate is set to 4µs • eBUS device is ready to receive a message
Test State	• PC sends a message to eBUS device • eBUS device sends message after SYN • LSA records messages • PC calculates time distance between start bit of SYN byte and bus permission of eBUS device • PC calculates length of start bit
Verification	• calculated time distance between start bit of SYN byte and bus permission must be in the range of: 4300µs ≤ time distance ≤ 4456,24µs • calculated length of start bit must be in the range: 411,18µs ≤ calculated length ≤ 421,16µs

The test:

Lower Tester	Flow	IUT eBUS Device
Set Up State according to definition above reached		
LSA_Starts_Recording(Signals_On_eBUS) PC_Sends(eBUS_Msg)		Dev_Receives(eBUS_ Msg) Dev_Sends_ Message(eBUS_IUT_Msg)
LSA_Stops_Recording(Signals_On_eBUS) PC_Filtering_SYN&StartBit(Signals_On_eBUS) PC_Calculates_Distance(SYN, StartBit) PC_Calculates_LengthOfStartBit(StartBit) PC_Checks(Calculated_Distance, Specified_Distance) PC_Checks(Calculated_LengthOfStartBit Specified_LengthOfStartBit		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	4300µs ≤ time distance ≤ 4456,24µs 411,18µs ≤ calculated length ≤ 421,16µs	measure result ± 4µs

Additional informations:

For this test LabView uses

- functions and procedures from eBUS.dll (Delphi) to set a trigger and to send messages to the eBUS device
- *timing.dll* (C) to filter bits from the measured values (stored in a text file) and to calculate the wanted times (see enclosure). The eBUS device sends messages with support of the Upper Tester software from the function tests, see document *eBUS Conformance Testing Layer 1 / 2, 1.0 - Function Tests*. The choosen function test has the number [2.1.2.1] in that document.

The test verdict is fail if one of the two expected test results is not in the permitted range.

4 AUTOSYN Generator

4.1 Static Test Current Consumption

IUT:
AUTOSYN generator

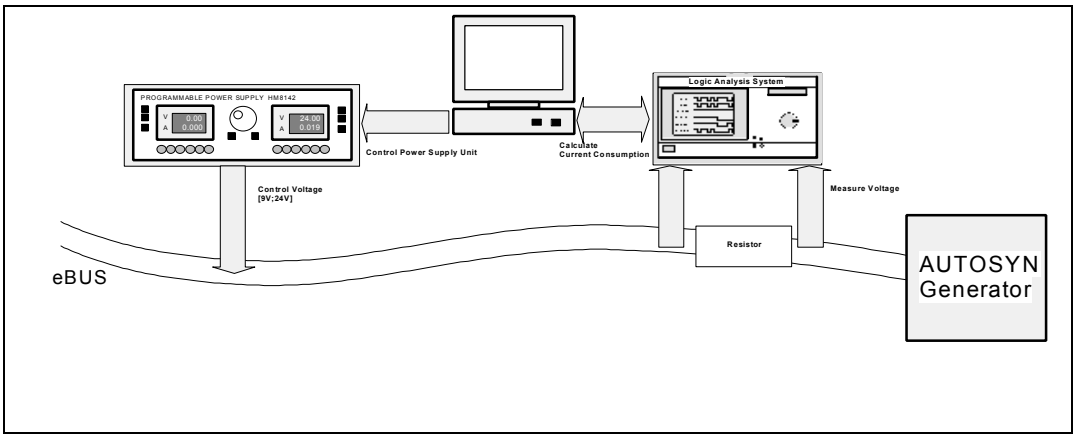


fig. 6 : current consumption of the AUTOSYN generator - used components of test environment

Purpose:
testing current consumption:
current consumption (low) ≤ current consumption (high) ≤ current consumption (low) + 10%

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • oscilloscope is initialized • oscilloscope is running
Test State	REPEAT IF measured voltage is in a specified range • oscilloscope records voltage • increment voltage UNTIL measured voltage is > 24V • PC calculates current consumption values from measured voltage values
Verification	• PC calculates CCL and CCH from extremes of measured values • calculated results should be: CCL ≤ CCH ≤ CCL + 10%

The test:

Lower Tester	Flow	IUT AUTOSYN Generator
Set Up State according to definition above reached		
REPEAT OSC_Measures_Voltage PC_Calculates_Curr_Cons(Voltage) INC_eBUS_Voltage UNTIL eBUS_Voltage ≥ Maximum PC_Calculates_Curr_Cons_L PC_Calculates_Curr_Cons_H PC_Checks(Calculated_Curr_Cons_L, Specified_Curr_Cons_L) PC_Checks(Calculated_Curr_Cons_H, Specified_Curr_Cons_H)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	CCL ≤ CCH ≤ CCL + 10%	Accuracy for voltage: 1,25% of full scale = 0,0125 · 4V + 0,016V / Div = 0,016V · 4 = 0,064 = 0,114V Accuracy for current consumption: 0,633mA

Additional informations:

The basic idea of this test is to measure the voltage at a certain point (measure point voltage, see sketch page 6) against grounding.
Depending on the law of Ohm and the fact that there is a resistor of 180Ω the current consumption can be calculated from the measured voltage in the following way:

$$U = R \cdot I \Rightarrow I = \frac{U}{R} \Rightarrow current\ consumption = \frac{measure\ result}{180\ \Omega}$$

For the verification the following values are taken from the measured values:
CCL = smallest value from the measured values which are specified as low level
CCH = biggest value from the measured values which are specified as high level

As a special result this test provides the value of the closed circuit consumption. For the eBUS system closed circuit consumption is defined as the current consumption of all nodes at high level.
Because in the given environment there is just one node the result for current consumption at high level is equivalent to the closed circuit consumption.

4.2 Dynamic Test Time Constraints for the AUTOSYN Byte

IUT:
AUTOSYN generator

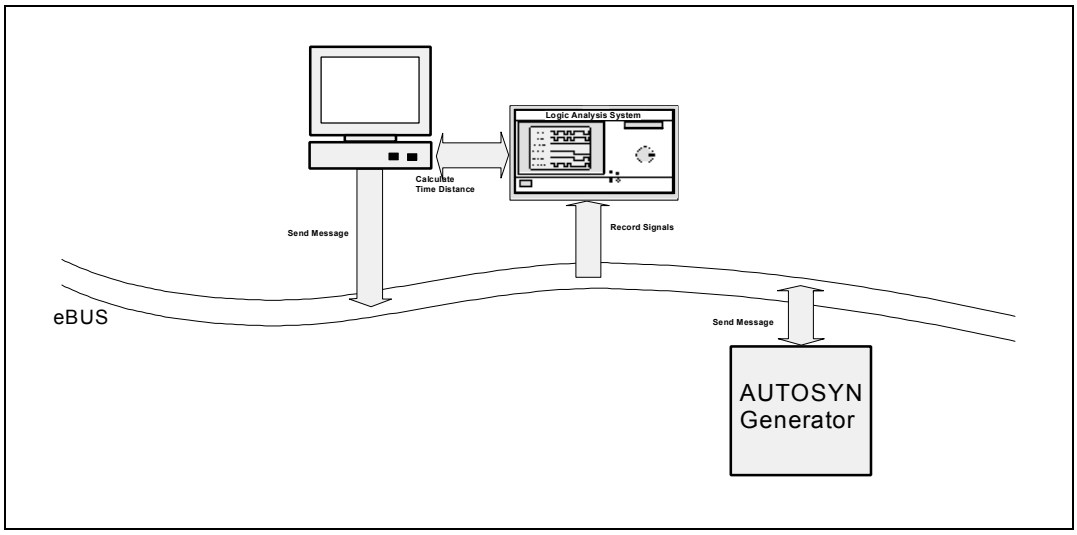
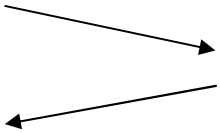


fig. 7 : time constraints for the AUTOSYN byte - used components of test environment

Purpose:
testing whether time distance between two AUTOSYN ≥ 30ms
testing whether time between a certain byte and the AUTOSYN ≥ 30ms

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • except AUTOSYN no signals on the eBUS • LSA is initialized • LSA is running • sample rate is set to 4µs
Test State	• AUTOSYN generator sends the signal AAh (AUTOSYN) • LSA records signal • PC calculates time SYN_SYN between two AUTOSYN • PC sends byte FFh • AUTOSYN generator sends the signal AAh • LSA records signal • PC calculates time BYTE_SYN between FFh and AAh
Verification	• SYN_SYN must be ≥ 30ms • BYTE_SYN must be ≥ 30ms

The test:

Lower Tester	Flow	IUT AUTOSYN Generator
Set Up State according to definition above reached manual settings done		
		AUTO_GEN_Sends(SYN_Signals)
LSA_Records(SYN_Signals) PC_Filtering_Two_SYN(Signals_On_eBUS) PC_Calculates_Distance(End_1.SYN, Start_2.SYN) PC_Calculates_Distance(Start_High, Start_SYN) PC_Checks(Calculated_Distances, Specified_Distance) PC_Sends_Byte		
		AUTO_GEN_Sends(SYN_Signals)
PC_Filtering_SYN_And_Byte(Signals_On_eBUS) PC_Calculates_Distance(End_Byte, Start_SYN) PC_Calculates_Distance(Start_High, Start_SYN) PC_Checks(Calculated_Distances, Specified_Distance)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	test result $\geq$ 30 ms	test result $\pm$ 4μs

Additional informations:

This test provides two results:

- time between start of high level in first byte and start of AUTOSYN
- time between end of stop bit of first byte and start of AUTOSYN (character oriented AUTOSYN generator)

For this test LabView uses

- functions and procedures from eBUS.dll (Delphi) to set a trigger
- *Byte.dll* (C) to filter bits from the measured values (stored in a text file) and to calculate the wanted times (see enclosure).

5 eBUS Transceiver

5.1 Static Tests

5.1.1 Static Test Current Consumption

IUT:
eBUS transceiver

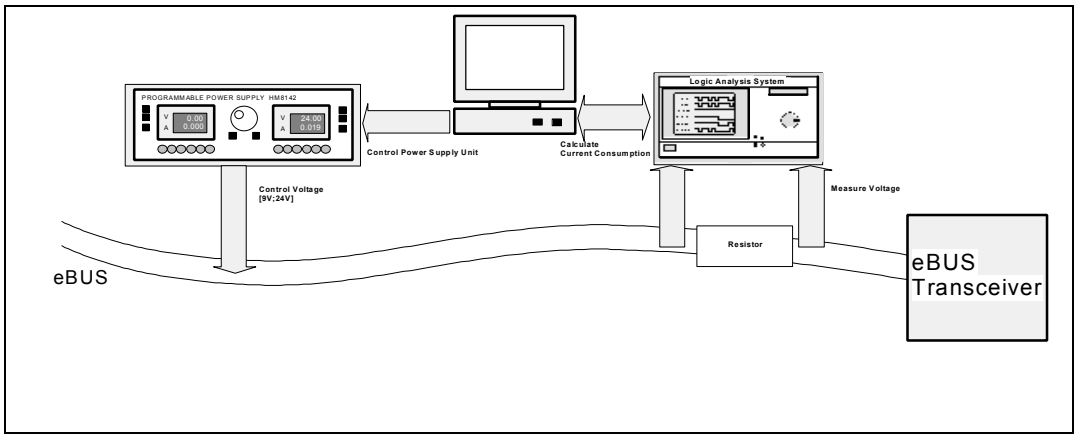


fig. 8 : current consumption of the eBUS transceiver - used components of test environment

Purpose:
testing current consumption:
current consumption (low) ≤ current consumption (high) ≤ current consumption (low) + 10%

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • oscilloscope is initialized • oscilloscope is running
Test State	REPEAT IF measured voltage is in a specified range • oscilloscope records voltage • increment voltage UNTIL measured voltage is > 24V • PC calculates current consumption values from measured voltage values
Verification	• PC calculates CCL and CCH from extremes of measured values • calculated results should be: CCL ≤ CCH ≤ CCL + 10%

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached REPEAT OSC_Measures_Voltage PC_Calculates_Curr_Cons(Voltage) INC_eBUS_Voltage UNTIL eBUS_Voltage ≥ Maximum PC_Calculates_Curr_Cons_L PC_Calculates_Curr_Cons_H PC_Checks(Calculated_Curr_Cons_L, Specified_Curr_Cons_L) PC_Checks(Calculated_Curr_Cons_H, Specified_Curr_Cons_H)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	CCL ≤ CCH ≤ CCL + 10%	Accuracy for voltage: 1,25% of full scale = 0,0125 · 4V + 0,016V / Div = 0,016V · 4 = 0,064 = 0,114V Accuracy for current consumption: 0,019mA

Additional informations:
The basic idea of this test is to measure the voltage at a certain point (measure point voltage, see sketch page 6) against grounding.
Depending on the law of Ohm and the fact that there is a resistor of 6kΩ the current consumption can be calculated from the measured voltage in the following way:

$$U = R \cdot I \Rightarrow I = \frac{U}{R} \Rightarrow current\ consumption = \frac{measure\ result}{6k\ \Omega}$$

For the verification the following values are taken from the measured values:
CCL = smallest value from the measured values which are specified as low level
CCH = biggest value from the measured values which are specified as high level

As a special result this test provides the value of the closed circuit consumption. For the eBUS system closed circuit consumption is defined as the current consumption of all nodes at high level.
Because in the given environment there is just one node the result for current consumption at high level is equivalent to the closed circuit consumption.

5.1.2 Static Test: Levels

IUT:
eBUS transceiver

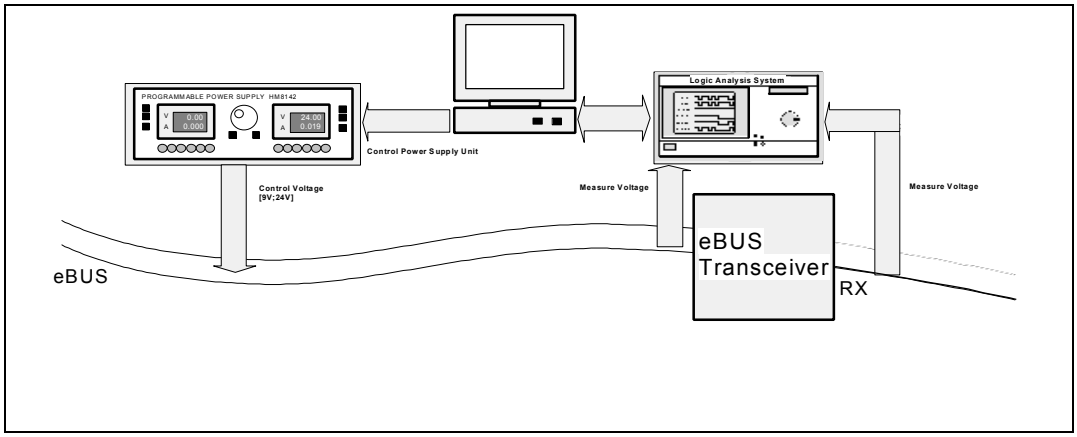


fig. 9 : RX - levels - used components of test environment

Purpose:
testing correct conversion from high level and low level at eBUS port of transceiver to high level and low level at serial outlet of the transceiver

State	Description
Set Up State	• power supply is adjusted to 9 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • oscilloscope is initialized • oscilloscope is running • sample rate is set to 200µs
Test State	REPEAT • oscilloscope records voltage at eBUS port of transceiver and at serial port of transceiver IF rising edge at serial port of transceiver: TRIGGER • increment voltage at eBUS port of transceiver UNTIL voltage at eBUS port ≥ 24V • oscilloscope measures threshold value (trigger) at eBUS port of transceiver • oscilloscope measures high level and low level at serial port of transceiver REPEAT • oscilloscope records voltage at eBUS port of transceiver and at serial port of transceiver IF rising edge at serial port of transceiver: TRIGGER • decrement voltage at eBUS port of transceiver UNTIL voltage at eBUS port < 9V • oscilloscope measures high level and low level at serial port of transceiver
Verification	calculated low/high level has to be in that range that is specified as logical 0/1 for the respective type of transceiver (see 'Additional informations')

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
REPEAT OSC_Records_Voltage_at_eBUS_Port_of_Transc OSC_Records_Voltage_at_serial_Port_of_Transc IF rising_edge_at_Serial_Port: Trigger INC_Voltage_at_eBUS_Port_of_Transc UNTIL Voltage_at_eBUS_Port > 24V OSC_Measures_Voltage_at_High_Level OSC_Measures_Voltage_at_Low_Level OSC_Measures_Threshold_Value_at_eBUS_Port REPEAT OSC_Records_Voltage_at_serial_Port_of_Transc OSC_Records_Voltage_at_eBUS_Port_of_Transc IF falling_edge_at_serial_Port: Trigger DEC_Voltage_at_eBUS_Port_of_Transc UNTIL Voltage_at_eBUS_Port < 9V OSC_Measures_Threshold_Value_at_eBUS_Port PC_Checks(Measured_High, Specified_High) PC_Checks(Measured_Low, Specified_Low)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	measured low level must be in the range specified as logical 0 measured high level must be in the range specified as logical 1	Accuracy for voltage: 1,25% of full scale = 0,0125 · 7,6V + 0,016V / Div = 0,016V · 4 = 0,064 = 0,159V

Additional Informations:

specified values for logical[1]	0	1
RS232 Input	-3V to -15V	3V to 15V
TTL Input Output	0V to 0,8V 0V to 0,4V	2V to 5V 2,4V to 5V

[1] from: Hans-Peter Messmer, 'PC-Hardwarebuch', Addison-Wesley 1992

5.1.3 Static Test : Bus Levels

IUT:
eBUS transceiver

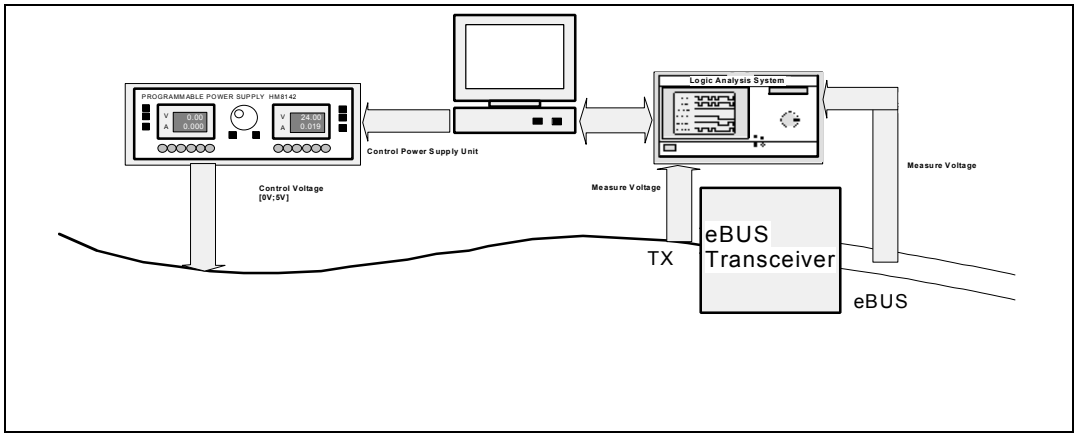


fig. 10 : TX - bus levels - used components of test environment

Purpose:
testing high level and low level of a sended signal at eBUS outlet of transceiver:
15 V < high level ≤ 24 V and 9 V ≤ low level ≤ 12 V

State	Description
Set Up State	• eBUS power supply is adjusted to the value which is specified as logical 1 for the respective transceiver type and the respective current value given at eBUS power supply (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • power supply unit is adjusted to the respective value which is specified as the logical 1 for the respective transceiver type • no signals on eBUS • oscilloscope initialized and oscilloscope running • sample rate is set to 200µs
Test State	REPEAT • oscilloscope records voltage at serial port of transceiver and voltage at eBUS port of transceiver IF falling edge at eBUS port: TRIGGER • decrement voltage at serial port of transceiver UNTIL voltage at serial port < minimum voltage • oscilloscope measures threshold value (trigger) at serial port of transceiver • oscilloscope measures high level and low level at eBUS port of transceiver REPEAT • oscilloscope records voltage at serial port of transceiver and voltage at eBUS port of transceiver IF rising edge at eBUS port: TRIGGER • increment voltage at serial port of transceiver UNTIL voltage at serial port > maximum voltage • oscilloscope measures threshold value (trigger) at serial port of transceiver
Verification	• calculated levels must be in the range of: 9 V ≤ measured low level ≤ 12 V

	15 V < measured high level ≤ 24 V

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
REPEAT OSC_Records_Voltage_at_serial_Port_of_Transc OSC_Records_Voltage_at_eBUS_Port_of_Transc IF falling_edge_at_eBUS_Port: Trigger DEC_Voltage_at_serial_Port_of_Transc UNTIL Voltage_at_serial_Port < Minimum OSC_Measures_Voltage_at_High_Level OSC_Measures_Voltage_at_Low_Level OSC_Measures_Threshold_Value_at_Serial_Port REPEAT OSC_Records_Voltage_at_serial_Port_of_Transc OSC_Records_Voltage_at_eBUS_Port_of_Transc IF rising_edge_at_eBUS_Port: Trigger INC_Voltage_at_serial_Port_of_Transc UNTIL Voltage_at_serial_Port > Maximum OSC_Measures_Threshold_Value_at_Serial_Port PC_Checks(Measured_High, Specified_High) PC_Checks(Measured_Low, Specified_Low)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	9 V ≤ measured low level ≤ 12 V 15 V < measured high level ≤ 24 V	Accuracy for voltage: 1,25% of full scale = 0,0125 · 40V + 1% · 5V + 2% · 40V + 0,016V / Div = 0,016V · 4 = 0,064 = 1,414V

5.2 Dynamic Tests TX

5.2.1 Rising Edges / Falling Edges

This test is executed without any electronic burden.

IUT:
eBUS transceiver

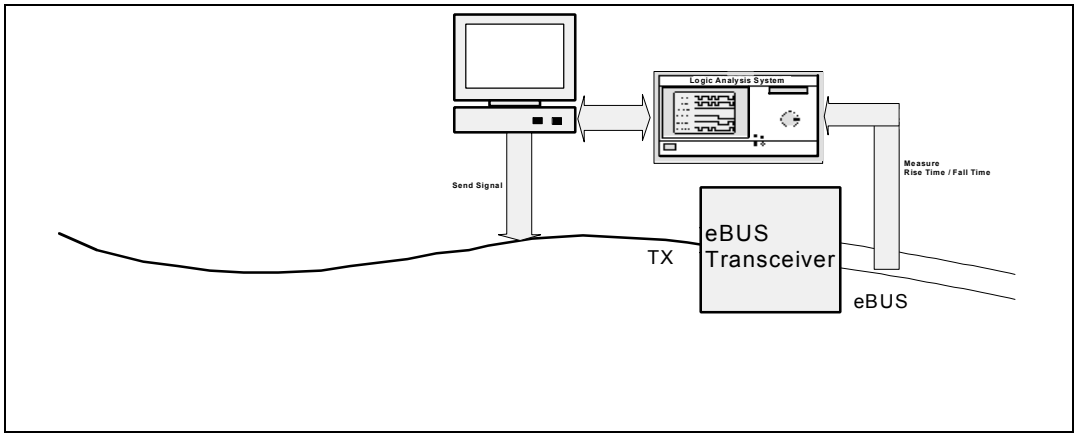


fig. 11 : TX - rising edges/falling edges - used components of test environment

Purpose:
testing rise time and fall time at eBUS outlet of transceiver:
rise time = fall time = 1/5 TQ = 5µs

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • serial interface is initialized to 2400 baud • oscilloscope is initialized • oscilloscope is running • sample rate is set to 400ns
Test State	• PC sends the signal 55h • oscilloscope records signal • oscilloscope measures rise time and fall time
Verification	• measured time for both rising and falling must be equal to 1/5 TQ = 5µs

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
PC_Sends(Signal)	→	TR_Converts_To_eBUS_Signal(Signal) TR_Sends(eBUS_Signal)
Osc_Records(eBUS_Signal) Osc_Measures_Rise_Time(eBUS_Signal) Osc_Measures_Fall_Time(eBUS_Signal)	←	
PC_Checks(Measured_Rise_Time, Specified_Rise_Time, Measured_Fall _ Time, Specified_Fall _ Time)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	1/5 TQ = 5µs	measure result ± 400ns

5.2.2 Transmitter : Delay Time

IUT:
eBUS transceiver

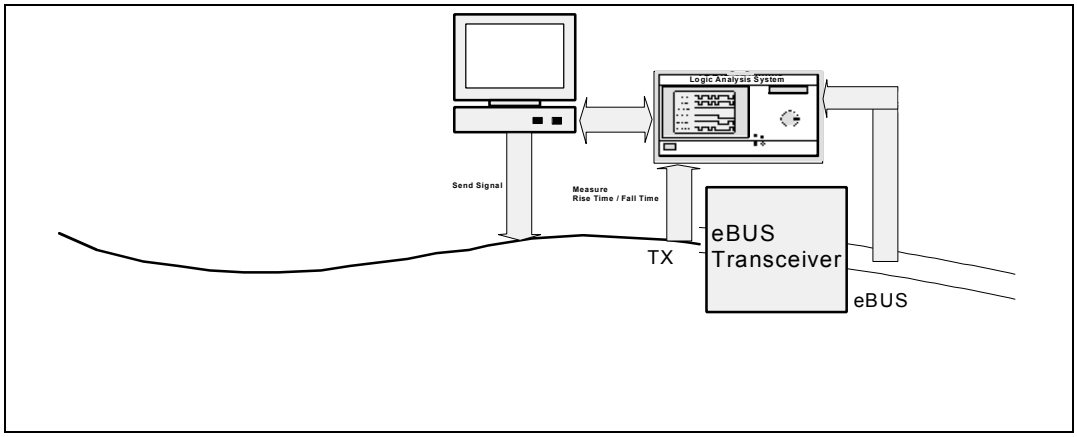


fig. 12 : TX - transmitter delay - used components of test environment

Purpose:
testing whether transmitter delay ≤ the respective product data given by the manufacturer

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • serial interface is initialized to 2400 baud • oscilloscope is initialized • oscilloscope is running • sample rate is set to 400ns
Test State	• PC sends the signal 55h • oscilloscope records signals at serial port of transceiver and at eBUS outlet of transceiver • oscilloscope measures time between the threshold value (from high to low) at serial port of transceiver and the respective threshold value at eBUS port of transceiver
Verification	• result should be ≤ the respective product data given by the manufacturer

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
PC_Sends(Signal) Osc_Records(Signal)	→	TR_Converts_To_eBUS_Signal(Signal) TR_Sends(eBUS_Signal)
Osc_Records(eBUS_Signal)	←	
Osc_Takes_Time1_of_Bit_x(Signal) Osc_Takes_Time2_Bit_x(eBUS_Signal)		
PC_Calculates_Delay(Time1, Time2) PC_Checks(Calculated_Delay, Specified_Delay)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	result ≤ the respective product data given by the manufacturer	measure result ± 400ns

5.3 Dynamic Tests RX

This test is executed without any electronic burden.

5.3.1 Rising Edges / Falling Edges

IUT:
eBUS transceiver

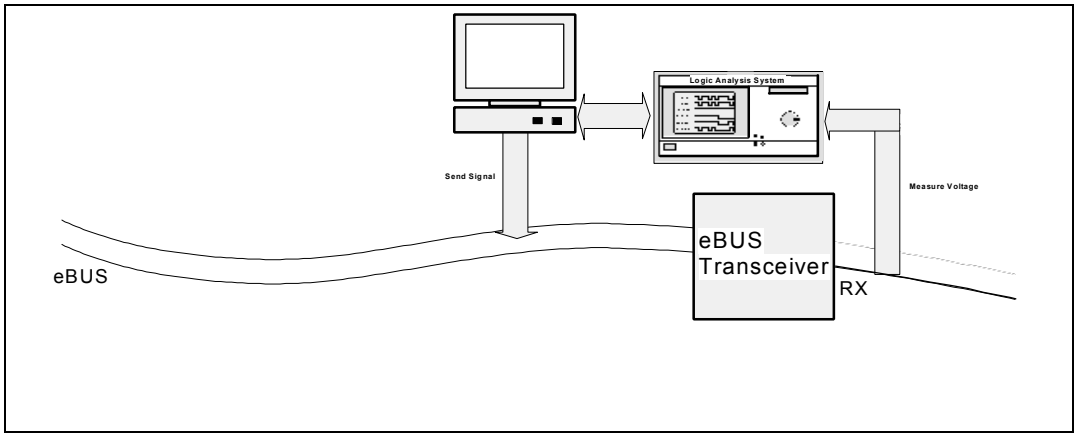


fig. 13 : RX - rising edges/falling edges - used components of test environment

Purpose:
testing rise time and fall time at serial outlet of eBUS transceiver:
rise time = fall time = 1/5 TQ = 5µs

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • serial interface is initialized to 2400 baud • oscilloscope is initialized • oscilloscope is running • sample rate is set to 400ns
Test State	• PC sends the signal 55h • oscilloscope records signal • oscilloscope measures rise time and fall time
Verification	• measured rise time = measured fall time must be equal to 1/5 TQ = 5µs

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
PC_Sends(eBUS_Signal)	→	TR_Receives(eBUS_Signal) TR_Converts_To_Signal(eBUS_Signal)
	←	
Osc_Records_Signal Osc_Measures_Rise_Time(Signal) Osc_Measures_Fall_Time(Signal)		
PC_Checks(Measured_Rise_Time, Specified_Rise_Time, Measured_Fall _ Time, Specified_Fall _ Time)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	1/5 TQ = 5µs	measure result ± 400ns

5.3.2 Receiver : Delay

IUT:
eBus Transceiver

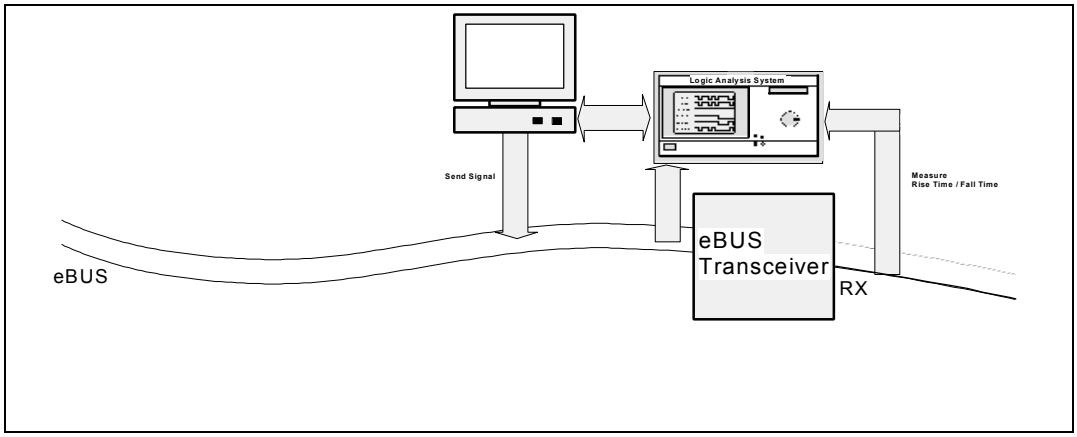


fig. 14 : RX - receiver delay - used components of test environment

Purpose:
testing whether receiver delay ≤ the respective product data given by the manufacturer

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • transceiver power supply is adjusted to 5 V • no signals on eBUS • serial interface is initialized to 2400 baud • oscilloscope is initialized • oscilloscope is running • sample rate is set to 400ns
Test State	• PC sends the signal 55h • oscilloscope records signals at serial port of the transceiver and at eBUS outlet of the transceiver • oscilloscope measures time between the threshold value (from high to low) at eBUS port of transceiver and the respective threshold value at serial port of transceiver
Verification	• result should be ≤ the respective product data given by the manufacturer

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
PC_Sends(eBUS_Signal)	→	
		TR_Receives(eBUS_Signal) TR_Converts_To_Signal(eBUS_Signal)
	←	
Osc_Records(eBUS_Signal) Osc_Takes_Time1_Bit_x(eBUS_Signal) Osc_Takes_Time2_Bit_x(Signal) PC_Calculates_Delay(StartTime1, StartTime2) PC_Checks(Calculated_Delay, Specified_Delay)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	result ≤ the respective product data given by the manufacturer	measure result ± 400ns

6 eBUS Power Supply

6.1 Maximum Voltage

IUT:
eBUS power supply

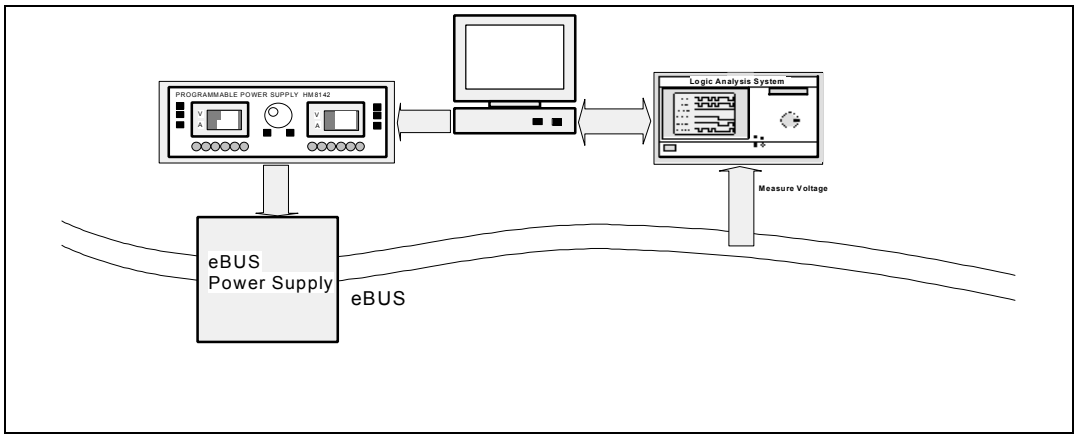


fig. 15 : eBUS power supply - maximum voltage - used components of test environment

Purpose:
testing whether maximum voltage ≤ 24V

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • no signals on eBUS • oscilloscope is initialized • oscilloscope is running
Test State	• oscilloscope measures voltage
Verification	• measured voltage must be less than or equal than 24 V

The test:

Lower Tester	Flow	IUT eBUS Transceiver
Set Up State according to definition above reached		
Osc_Measures_Voltage PC_Checks(Measured_Voltage, Specified_Voltage)		

Test analysis and results:

Number of Iterations	Expected Result According to Specification	Accuracy
5	result ≤ 24 V	Accuracy for voltage: 1,25% of full scale = 0,0125 · 20V + 0,016V/Div = 0,016 · 4 = 0,064 = 0,314V

6.2 Entire Current

IUT:
eBUS power supply

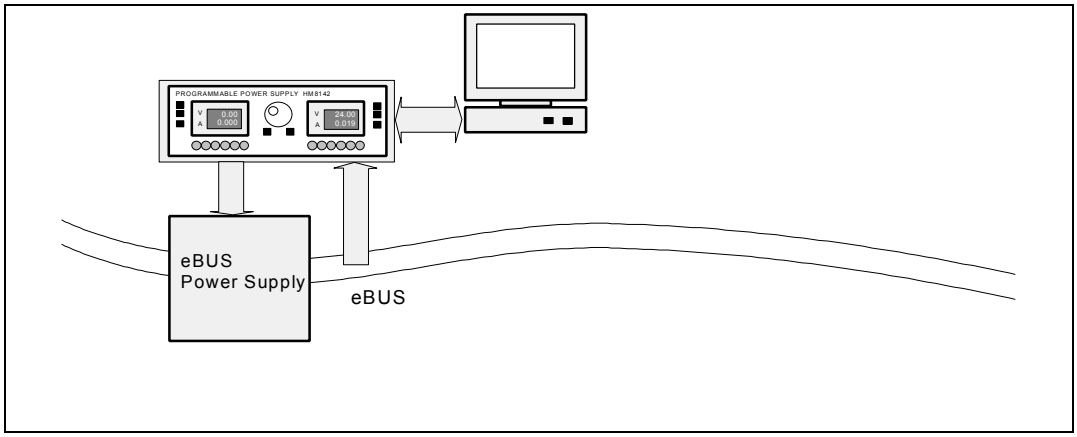


fig. 16 : eBUS power supply – entire current - used components of test environment

Purpose:
testing whether the short circuit is in the range specified at the eBUS power supply to be tested

State	Description
Set Up State	• power supply is adjusted to 24 V and the respective current value given at eBUS power supply unit (30mA ≤ I ≤ 100mA) • additional power supply unit is adjusted to 0 V and 0mA • no signals on eBUS
Test State	REPEAT • PC reads measured eBUS voltage from additional power supply unit • PC reads current value from additional power supply unit • increment current value at additional power supply unit UNTIL current value > 100mA
Verification	measured eBUS voltage must be HIGH for all current values ≤ current value given at eBUS power supply and must be ≠ HIGH for all current values > current value given at eBUS power supply

The test:

Lower Tester	Flow	IUT eBUS Power Supply
Set Up State according to definition above reached		
REPEAT PC_Reads_Voltage(Additional_Power_Supply) PC_Reads_Current(Additional_Power_Supply) INC_Current(Additional_Power_Supply) UNTIL Current > 100mA		

Test analysis and results:

Number of Iterations	Expected Result	Accuracy
5	measured eBUS voltage must equal HIGH for all current values ≤ current value given at eBUS power supply and must be ≠ HIGH for current values > current value given at eBUS power supply	Accuracy of voltage: 0,02% of measured value ± 1 digit

7 Appendix

7.1 Check List

7.1.1 Devices Realized as Separate Devices

Test	eBUS Device	eBUS Power Supply	AUTOSYN Generator	eBUS Transceiver
3.1	**x** • manufacturers specific range must be given • test is not necessary to gain the 'pass' verdict	-	-	-
3.2	**x**	-	-	-
4.1	-	-	**x** • manufacturers specific range must be given • test is not necessary to gain the 'pass' verdict	-
4.2	-	-	x	x
5.1.1	-	-	-	**x** • manufacturers specific range must be given • test is not necessary to gain the 'pass' verdict
5.1.2	-	-	-	**x**
5.1.3	-	-	-	**x**
5.2.1	-	-	-	**x**
5.2.2	-	-	-	**x** • manufacturers specific delay time must be given • test is not necessary to gain the 'pass' verdict
5.3.1	-	-	-	**x**
5.3.2	-	-	-	**x** • manufacturers specific delay time must be given • test is not necessary to gain the 'pass' verdict
6.1	-	**x**	-	-
6.2	-	**x**	-	-

7.1.2 Devices Realized as Combinations

Test	eBUS Device in Combination with any other Device (e.g. AUTOSYN Generator, eBUS Power Supply)	eBUS Power Supply in Combination with any other Device (e.g. AUTOSYN Generator, eBUS Device)	AUTOSYN Generator in Combination with any other Device (e.g. eBUS Device, eBUS Power Supply)	eBUS Transceiver in Combination with eBUS Device and possibly other Devices (e.g. AUTOSYN Generator)
3.1	• manufacturers specific range must be given • must be prepared in a way that the devices can be separated • test is not necessary to gain the 'pass' verdict	-	-	-
3.2	**x**	-	-	-
4.1	-	-	• manufacturers specific range must be given • must be prepared in a way that the devices can be separated • test is not necessary to gain the 'pass' verdict	-
4.2	-	-	**x**	-
5.1.1	-	-	-	• manufacturers specific range must be given • must be prepared in a way that the devices can be separated • test is not necessary to gain the 'pass' verdict
5.1.2	-	-	-	RX and TX pins must be accessible
5.1.3	-	-	-	RX and TX pins must be accessible
5.2.1	-	-	-	RX and TX pins must be accessible
5.2.2	-	-	-	• RX and TX pins must be accessible • manufacturer specific delay time must be given • test is not necessary to gain the 'pass' verdict
5.3.1	-	-	-	RX and TX pins must be accessible
5.3.2	-	-	-	• RX and TX pins must be accessible • manufacturers specific delay time must be given • test is not necessary to gain the 'pass' verdict
6.1	-	must be prepared in away that the devices can be separated	-	-
6.2	-	must be prepared in a way that the devices can be separated	-	-

7.2 Survey: Expected Measure Results

eBUS Device Under Test		
3.1	Current Consumption	1 mA ≤ CCL ≤ 5 mA CCL ≤ CCH ≤ CCL + 10%
3.2	Bus Permission after SYN Byte Length of the Start Bit	4300µs ≤ time distance ≤ (4300 + 156,24) µs length of start bit ≥ 411µs
AUTOSYN Generator Under Test		
3.1	Current Consumption	1 mA ≤ CCL ≤ 5 mA CCL ≤ CCH ≤ CCL + 10%
3.2	Time Constraints for AUTOSYN Byte	result ≥ 30ms
eBUS Transceiver Under Test		
5.1.1	Static Test : Current Consumption	calculated results must be: CCL ≤ CCH ≤ CCL + 10%
5.1.2	Static Test : Levels	RS232: -15 V ≤ low result ≤ -5 V 5 V ≤ high result ≤ 15 V TTL : 0 V ≤ low result ≤ 0,5 V 2,5 V ≤ high result ≤ 5 V
5.1.3	Static Test : Bus Levels	9 V ≤ low level ≤ 12 V 15 V < high level ≤ 24 V
5.2.1	TX – Rising Edges/Falling Edges	1/5 TQ = 5 µs
5.2.2	TX – Transmitter: Delay Time	result ≤ 20 µs
5.3.1	RX – Rising Edges/Falling Edges	1/5 TQ = 5µs
5.3.2	RX – Receiver: Delay	result ≤ 20µs
eBUS Power Supply Under Test		
6.1	Maximum Voltage	result ≤ 24 V
6.2	Entire Current	measured eBUS voltage must be HIGH for all current values ≤ current value given at eBUS power supply and must be ≠ HIGH for current values > current value given at eBUS power supply

7.3 Abbrevations

CCH	current consumption at high level
CCL	current consumption at low level
GND	ground
GPIB	General Purpose Interface Bus (ANSI/IEEE Standard 488.1-1987)
IUT	implementation under test
LSA	logic state analyzer
LT	lower tester
RX	receive data
TQ	time quantum
TX	transmit data
UT	upper tester

7.4 List of Figures

8 Änderungsliste

Version	Datum	Bemerkungen	
1.1	1998	Initial Version	Frank Hoffmann
1.1.1	03.2007	Änderung der eBUS User Club Logos nach eBUS Interest Group	Frank Hoffmann